PATENT ABSTRACTS OF JAPAN

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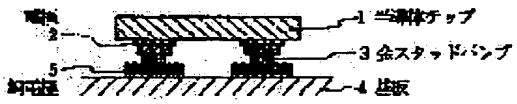
(54) FLIP-CHIP MOUNTING STRUCTURE AND MANUFACTURE THEREOF

(57)Abstract:
PROBLEM TO BE SOLVED: To lessen the man-hours of the manufacture of a flip-chip mounting structure to aim at preventing the defective connection of a semiconductor chip with a substrate, a bridge and the like from being generated and to enhance the reliability of the connection of the chip with the substrate.
SOLUTION: Metal stud bumps 3 are formed on electrodes 2 on a semiconductor chip 1, and the surfaces of copper electrodes 5 on a substrate 4 are subjected to plasma treatment for cleaning and activating the surfaces of the electrodes 5. The pointed parts of the bumps 3 are pressed to the surfaces, which were subjected to plasma treatment of the electrodes 5 to heat-treat the pointed parts of the bumps 3 at a temperature of 250° C or thereabouts and the gold constituting the bumps 3 is made to react directly with the copper constituting the electrodes 5 for bonding the bumps 3 to the electrodes 5.



LEGAL STATUS

[Date of request for examination]

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CLAIMS

[Claim(s)]
[Claim 1] Flip chip mounting structure where the golden stud bump formed on the electrode of a bare chip and the copper electrode of the substrate defecated and activated by plasma treatment are characterized by being joined directly in the flip chip mounting structure of mounting a bare chip directly on a substrate.
[Claim 2] The manufacture method of the flip chip mounting structure which is the manufacture method of the flip chip mounting structure of a claim 1, and is characterized by having the process which forms a golden stud bump on the electrode of a bare chip, the plasma treatment process for defecating and activating the front face of the copper electrode on a substrate, and the junction process which joins the golden stud bump of a bare chip to the front face of the copper electrode by which plasma treatment was carried out directly.
[Claim 3] per [as opposed to / the plasma treatment of the aforementioned plasma treatment process is the plasma treatment by argon gas or hydrogen gas, the atmosphere of the aforementioned junction process is among air or an inert atmosphere, and junction temperature is 230 - 270 **, and / the last plane-of-composition product] unit area -- a load -- 3-10kg/mm2 it is -- the manufacture method of the flip chip mounting structure according to claim 2 characterized by being a pressurization heat treatment process

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[The technical field to which invention belongs] This invention relates to the flip chip mounting structure and its manufacture method of a bare chip to a substrate.
[0002]
[Description of the Prior Art] The following two methods are adopted in the conventional flip chip mounting. The 1 is a method by soldering. This method is the method of heat-treating and soldering, where it formed the golden stud bump 3 on the front face of the electrode 2 of the semiconductor bare chip (it sets to drawing and is a semiconductor chip) 1, it supplied cream solder by screen-stencil on the copper electrode 5 of a substrate 4 and both are contacted, as shown in drawing 3 .
[0003] Since the presswork of cream solder is required of this method, a process is complicated and there are many man days. Moreover, an inter-electrode pitch is 200. mum If it becomes the following ** pitches, since printing will become difficult, the method of carrying out the precoat of the solder directly is needed for a substrate 4. However, control of the amount of solder is difficult, for the reason, poor junction, a bridge, etc. are generated and the high rate of an excellent article is not obtained.
[0004] The 2 is a method by the anisotropy electric conduction film (below, it is called ACF for short) or the electroconductive glue. The method by ACF is the method of forming the golden stud bump 3 on the electrode 2 of the semiconductor bare chip 1, or forming a copper bump etc. by plating, being in the state which sandwiched ACF7 between this golden stud bump 3 grade and the copper electrode 5 of a substrate 4, heat-treating, and making both switch-on, and joining, as shown in drawing 4 .
[0005] In the case of an electroconductive glue, an electroconductive glue is supplied by screen-stencil on the copper electrode 5 of a substrate 4, and between golden stud bump 3 grade and the copper electrodes 5 of a substrate 4 is joined by the conductive state by the electroconductive glue.
[0006] Since ACF and an electroconductive glue mix a conductive filler in adhesives, it depends for the conductivity on contact between fillers. Therefore, if influenced of thermal stress, it has the problem that connection reliability falls.
[0007]
[Problem(s) to be Solved by the Invention] The technical problem of this invention is generating neither a faulty connection nor a bridge, and offering the flip chip mounting structure connection reliability's being high, and its manufacture method, even if the manufacturing process which canceled the trouble in the above-mentioned conventional technology is simple and an inter-electrode pitch becomes narrow.
[0008]
[Means for Solving the Problem] In this invention, the golden stud bump formed on the electrode of a bare chip and the copper electrode of the substrate defecated and activated by plasma treatment are directly joined in the flip chip mounting structure of mounting a bare chip directly on a substrate (invention of a claim 1).

[0009] Since foreign matters, such as dirt and an oxidizing zone, do not exist, comparatively, at low temperature, the direct reaction of the copper electrode and golden stud PAMPU which were processed is easily carried out to the front face of the copper electrode defecated and activated by plasma treatment, and they are joined to it. And in this structure, there are no restrictions on a size which is followed on a screen-stencil process or a soldered joint process.
[0010] Next, next it is the manufacture method of the flip chip mounting structure of a claim 1, and is equipped with the process which forms a golden stud bump on the electrode of a bare chip, the plasma treatment process for defecating and activating the front face of the copper electrode on a substrate, and the junction process which joins the golden stud bump of a bare chip to the front face of the copper electrode by which plasma treatment was carried out directly (invention of a claim 2).
[0011] In a golden stud bump's formation process, and a plasma treatment process and the direct junction process of a copper electrode and a golden stud bump, there are no restrictions on a size like the screen-stencil process in the conventional technology or a soldered joint process, and its process is also simple at them.
[0012] per [as opposed to / in the manufacture method of the flip chip mounting structure of a claim 2, the plasma treatment of the aforementioned plasma treatment process is the plasma treatment by argon gas or hydrogen gas, the atmosphere of the aforementioned junction process is among air or an inert atmosphere, and junction temperature is 230-270 **, and / the last plane-of-composition product] unit area -- a load -- 3-10kg/mm2 it is -- it is a pressurization heat treatment process (invention of a claim 3) Such a plasma treatment process and a pressurization heat treatment process are down stream processing which both can carry out easily in the present technical level.
[0013]
[Embodiments of the Invention] The gestalt of operation of the flip chip mounting structure by this invention and its manufacture method is explained using an example. In addition, the same sign was given to the portion of the same function as the conventional technology.
[0014] Drawing 1 is the cross section showing the structure of the example of the flip chip mounting structure by this invention, drawing 2 shows the example of the manufacture method, and the cross section in which (a) shows the state in front of junction, and (b) are the cross sections showing the state in the middle of junction.
[0015] The golden stud bump 3 by whom the example of this flip chip mounting structure was formed on the electrode 2 of ******** ACHIPPU (it sets to drawing and is a semiconductor chip) 1, and the copper electrode 5 of a substrate 4 are joined directly. Both can join directly because the plasma treatment which used argon gas defecates the front face of a copper electrode 5 and it is activated.
[0016] 0.1 Torr and the processing time come [RF power density / 400 W/900cm2 and argon gas pressure] out of the conditions of this plasma treatment for 60 seconds This processing is processing which removes the copper oxide currently generated by dirt and front faces, such as the organic substance which accelerated the argon ion generated in plasma by electric field, was made to collide with the front face of a copper electrode 5, and has adhered to the front face of a copper electrode 5. By this processing, the front face of a copper electrode 5 turns into the plasma treatment side 51 defecated and activated. Since the copper oxide currently generated by dirt and front faces, such as the organic substance adhering to the front face of a copper electrode 5, checks the direct junction to the golden stud bump 3 and a copper electrode 5, it is important for it to remove these.
[0017] The golden stud bump 3 is 32 micrometers of wire sizes. After a gold streak can add a 10g load for 30 seconds by 250 ** and is joined to an electrode 2, it is perpendicularly torn off by the electrode 2 and is fabricated by the configuration where the nose of cam as shown in drawing sharpened.
[0018] The junction process of the copper electrode 5 of a substrate 4 and the golden stud bump 3 of the semiconductor bare chip 1 is a process which controls the temperature of the fixture holding the semiconductor bare chip 1, heats the semiconductor bare chip 1 to predetermined temperature, and pushes the golden stud bump 3 with this fixture while controlling

a load to a copper electrode 5. A substrate 4 is not heated for maintaining the surface state of the copper electrode 5 which plasma treatment defecated, and it is joinable into air with this effect. In addition, if junction atmosphere is made into inert gas atmosphere, the surface state of the copper electrode 5 by plasma treatment is more maintainable for a long time.
[0019] In a junction process, the copper electrode 5 by which the portion into which the golden stud bump 3 sharpened was defecated and activated by plasma treatment is contacted, when the point eats away in a copper electrode 5, a copper new field is exposed and a copper new field and copper gold contact. Consequently, the counter diffusion of gold and copper fully advances and a suitable junction state is acquired. The portion into which the golden stud bump 3 sharpened eats away in a copper electrode 5 because the front face of a copper electrode 5 is defecated and activated by plasma treatment in addition to a load concentrating on the small area at a tip. CuAu3 which is the intermetallic compound of gold and copper at the portion from which gold and copper carried out counter diffusion, and changed into the suitable junction state What is formed is presumed.
[0020] Drawing 2 (a) shows the state just before the portion into which the golden stud bump 3 sharpened contacts the plasma treatment side 51 of a copper electrode 5, and the portion into which (b) sharpened eats into a copper electrode 5 partly, and it shows the state where the bump interlocking section 52 is seen. If heating temperature of the semiconductor bare chip 1 is made into 230 ** to 270 **, a load is made into 10-20g / bump and the load holding time is set as for 30 seconds, interlocking, deformation, and counter diffusion will be in the state which it goes on moderately and shows in drawing 1 , and perfect junction will be completed. A final area for a joint is phi50-60micrometer. It is a grade and is 2 3-10kg/mm as a load per unit area. It becomes. However, in the early stages of junction, since only the golden stud bump's 3 tip contacts a copper electrode 5, the load per unit area serves as a far bigger value than this. If under 10g / bump, or heating temperature becomes under 230 **, deformation and reacting the aforementioned load for a joint will become inadequate, sufficient junction cannot be performed, and if 20g / excess of a bump, or heating temperature becomes an excess of 270 **, it will become superfluous the golden stud bump's 3 deforming a load.
[0021] According to this example, poor junction and the bridge were not generated but have realized reliable flip chip mounting. In addition, in the above-mentioned example, although the case where flip chip mounting of the semiconductor bare chip 1 was carried out at a substrate 4 was explained, it is effective similarly to bare chips other than a semiconductor. Moreover, in the above-mentioned example, although the plasma treatment by argon gas was explained, the reactant plasma treatment using hydrogen gas is effective similarly.
[0022]
[Effect of the Invention] According to this invention, in the flip chip mounting structure of mounting a bare chip directly on a substrate, the golden stud bump formed on the electrode of a bare chip and the copper electrode of the substrate defecated and activated by plasma treatment are joined directly. Since foreign matters, such as dirt and an oxidizing zone, do not exist, comparatively, at low temperature, the direct reaction of the copper electrode and golden stud PAMPU which were processed is easily carried out to the front face of the copper electrode defecated and activated by plasma treatment, and they are joined to it. And in this structure, there are no restrictions on a size which is followed on a screen-stencil process or a soldered joint process. Therefore, even if a manufacturing process is simple and an inter-electrode pitch becomes narrow, neither a faulty connection nor a bridge is generated, and the flip chip mounting structure where connection reliability is high can be offered (invention of a claim 1).
[0023] Next, next it is the manufacture method of the flip chip mounting structure of a claim 1, and is equipped with the process which forms a golden stud bump on the electrode of a bare chip, the plasma treatment process for defecating and activating the front face of the copper electrode on a substrate, and the process which joins the golden stud bump of ** ACHIPPU to the front face of the copper electrode by which plasma treatment was carried out directly. In a golden stud bump's formation process, and a plasma treatment process and the direct junction process of a copper electrode and a golden stud bump, there are no restrictions on a size like

the screen-stencil process in the conventional technology or a soldered joint process, and its process is also simple at them. Therefore, even if a manufacturing process is simple and an inter-electrode pitch becomes narrow, neither a faulty connection nor a bridge is generated, and the manufacture method of the flip chip mounting structure where connection reliability is high can be offered (invention of a claim 2).

[0024] per [as opposed to / in the manufacture method of the flip chip mounting structure of a claim 2, a plasma treatment process is a plasma treatment process by argon gas or hydrogen gas, the atmosphere of a junction process is among air or an inert atmosphere, and junction temperature is 230 - 270 **, and / the last plane-of-composition product] unit area -- a load -- 3-10kg/mm2 it is -- it is a pressurization heat treatment process Such a plasma treatment process and a pressurization heat treatment process are down stream processing which both can carry out easily in the present technical level. Therefore, the technical problem of this invention can be attained certainly easily (invention of a claim 3).

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DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] The cross section showing the structure of the example of the flip chip mounting structure by this invention
[Drawing 2] It is the cross section in which the cross section in which (a) shows the state in front of junction, and (b) show the state in the middle of junction by showing the example of the manufacture method of the flip chip mounting structure by this invention.
[Drawing 3] The cross section showing an example of the flip chip mounting method by the conventional technology
[Drawing 4] The cross section showing the other examples of the flip chip mounting method by the conventional technology
[Description of Notations]
1 Semiconductor Chip 2 Electrode
3 Golden Stud Bump 4 Substrate
5 Copper Electrode 51 Plasma Treatment Side
52 Bump Interlocking Section
6 Cream Solder 7 ACF

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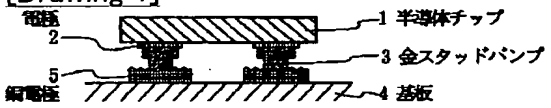
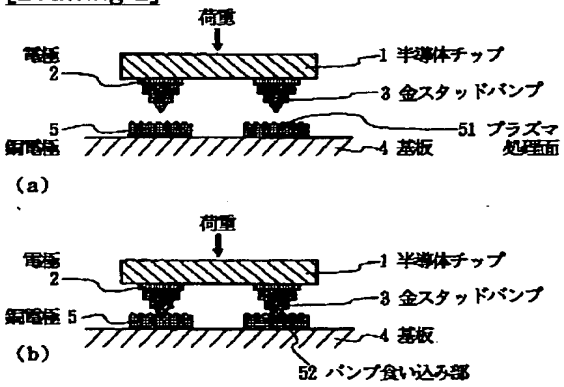
DRAWINGS

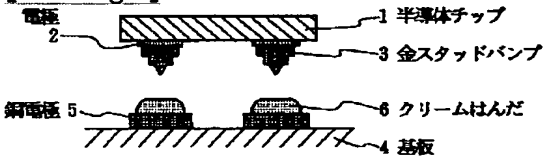
[Drawing 1]



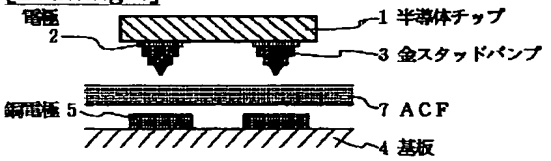
[Drawing 2]



[Drawing 3]



[Drawing 4]



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